REMARKS

A drawing amendment is attached wherein Fig. 4 is designated as "prior art".

The length of the Abstract of the Disclosure has been shortened to make the Abstract less than 150 words. A typographical error has also been corrected in the Specification.

Claims 10, 15 and 20 were amended to correct a typographical error, and to remove references to "steps of". These amendments were not made for a reason related to the patentability of these claims, and the full range of equivalents for all of the pending claims should remain intact.

Claims 1, 2, 6-11, 15-18, 20-22 and 24 have been rejected under 35 U.S.C. 103(a) as being obvious over Matsuo et al. (U.S. 5,301,137) in view of Aldrich et al. (U.S. 6,601,077), and claims 3-5, 12-14, 19 and 23 have been rejected under 35 U.S.C. 103(a) as being obvious over Matsuo et al. in view of Aldrich et al., as applied to claim 1, and further in view of Cheung et al. (U.S. 6,369,610). These rejections are respectfully disagreed with, and are traversed below.

Claim 1 recites, in part, that a data processor includes:

> "a multiplier block having a multiplier front end for generating partial products from input operands; and a plurality of arithmetic logic units (ALUs) having inputs switchably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUs being switchably coupled, in a second mode of operation, to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources" (emphasis added).

First, it is respectfully submitted that Fig. 1 of Matsuo et al. does not show or suggest a "plurality of arithmetic logic units (106)" as stated by the Examiner on page 3, Section 5, lines 5 and 6. Fig. 1 shows only a single ALU 106, as do the Figures 4, 6 and 7. Col. 1, line 48, to col. 2, line 8, refer to "an arithmetic logic unit (ALU) 106", and to "the ALU 106" (only the singular case, not the plural case, is referred to).

The Examiner then states that Matsuo et al. do not disclose explicitly in Figure 1 a plurality of ALUs, and uses Aldrich et al. for disclosing in Figure 3 that an ALU (165) is composed of several small ALUs (378 and 380). The Examiner then states that it would have been obvious to add the plurality of ALUs of Aldrich et al. to Matsuo et al.

It is pointed out that there is in actuality a single data source in Matsuo et al., that is, the input registers 101 and 102. As is stated at col. 1, lines 27-34, whether the multiplier 103 executes fixed point or floating point operations is based on the mode control signal 202. The operation of the ALU 106 is determined by decoder 108, and executes an operation determined by the control signal 109 with the outputs of selectors 104 and 105. The inputs to the selectors 104 and 105 do not represent two data sources, but appear to be derived either directly from the input registers 101, 102, or indirectly via multiplier 103 (selector 104) and the accumulator 107 at the output of the ALU 106, via selector 105.

For at least these reasons, it is respectfully submitted that Matsuo et al. do not disclose or suggest at least the subject matter highlighted above.

Turning now to Aldrich et al., what is disclosed appears to be a multi-stage (three stage) pipelined processing unit optimized for pixel processing, more specifically one optimized for performing sum of absolute difference (SAD) calculations for pixel pairs (see col. 3, lines 10-40). In the embodiments of Figs. 2, 3, 4 and 5 it appears that the pixel pair SAD values are computed in the first stage, they are combined in the second stage, and the third stage accumulates these combined values over an image frame.

Although it is not admitted that there is any suggestion in a reading of these two U.S. Patents that they could be combined in the manner done by the Examiner, it is clear that if one replaced the ALU 106 of Matsuo et al. with the ALU 165 of Fig. 3 (or Fig. 5) of Aldrich et al., that contains two ALUs 378, 380, the resulting modified system would still suffer from the shortcomings present in the Matsuo et al. system, as was discussed above. Further, it is not seen where Aldrich et al. cure these shortcomings by teaching or suggesting, as in claim 1, that a plurality of ALUs

have inputs switchably coupled, in a first mode of operation, to first data sources comprised of outputs of a multiplier front end for adding together partial products or, in a second mode of operation, to second data sources for performing at least one of arithmetic and logical operations on data received from the second data sources.

Claim 1 is thus clearly patentable over the proposed combination of Matsuo et al. and Aldrich et al.

The foregoing argument applies as well to method independent claim 10, that recites in part (as amended above to correct a simple typographical error):

> "providing said multiplier block with a plurality of arithmetic logic units (ALUs); wherein
>
> in a first mode of operation, said plurality of ALUs have inputs switchably coupled to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result; and
>
> in a second mode of operation, said inputs of said plurality of ALUs are switchably coupled to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources."

Furthermore, independent claim 21 is drawn to a DSP and recites in part that the DSP includes a:

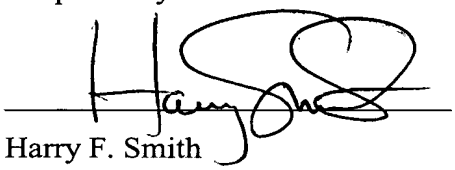
> "multiplier block further comprising circuitry for adding together said partial products, said circuitry comprising a plurality of ALUs having inputs that are programmably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUs being programmably coupled, in a second mode of operation, to second data sources for selectively operating together in parallel for performing at least one of arithmetic and logical operations on data received from said second data sources".

It is respectfully submitted that the independent claims 1, 10 and 15 are all patentably distinct

from the Examiner's proposed combination of Matsuo et al. and Aldrich et al. Since this is true, then all of the dependent claims are patentable as well, whether or not they are considered with the additional disclosure of Cheung et al., at least for the reason that each depends either directly or indirectly from an allowable independent claim.

The Examiner is respectfully requested to reconsider and remove the rejections, and to allow the claims as presented above. An early notification of the allowance of claims 1-24 is earnestly solicited.

Respectfully submitted:



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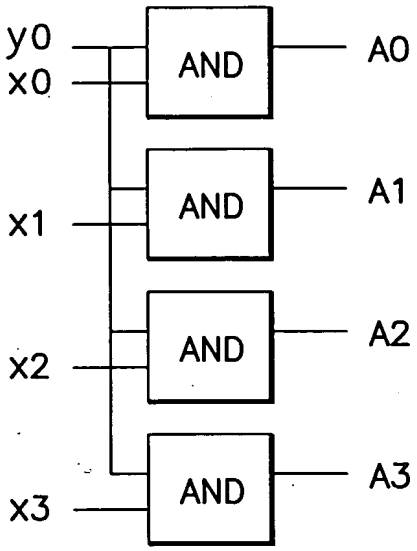
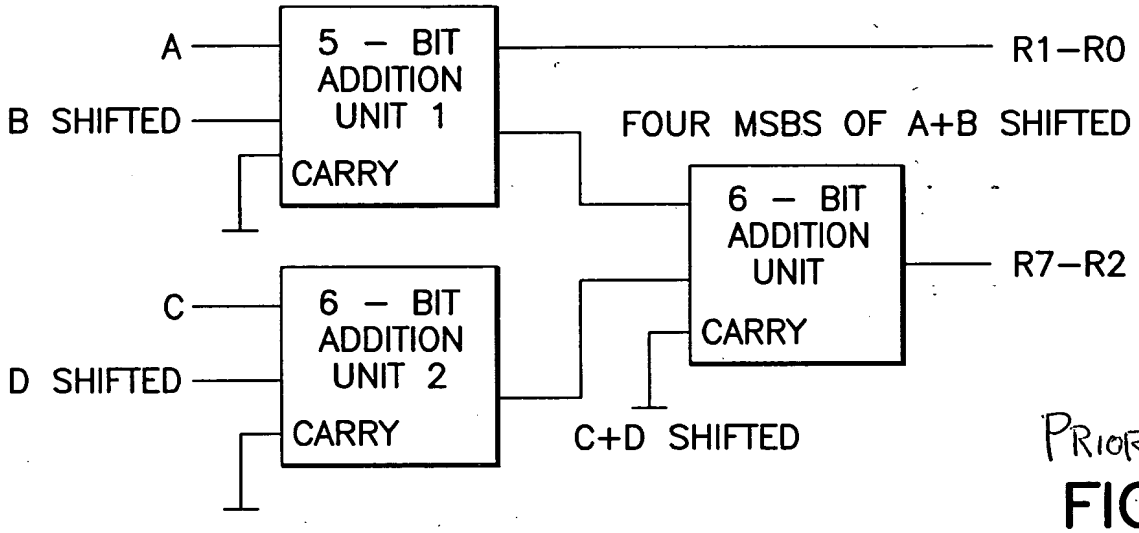


FIG.3



PRIOR ART

FIG.4

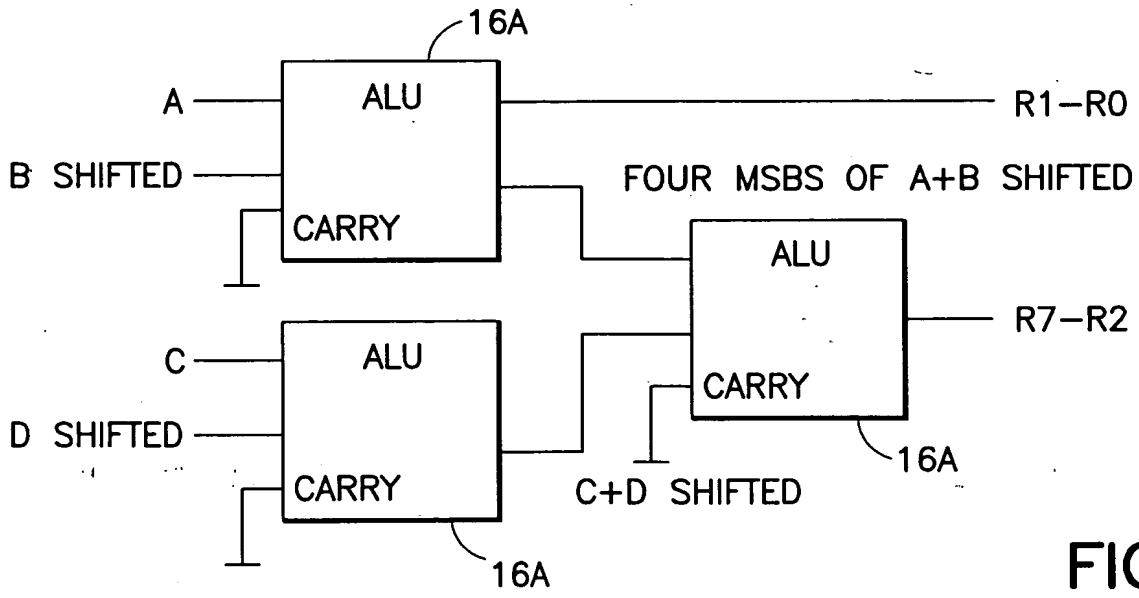


FIG.5